# Design and Analysis of Encoder and Decoder for Golay Code

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**Abstract:** A binary Golay code is a type of linear error correcting code used in digital communications. The two binary Golay codes formats are the Binary Golay Code G23 and Extended Binary Golay code (G24). The Golay code encodes 12-bits of data in such a way that it can correct 3-bits of error and detect 7-bits of error. G24 code is also called the Perfect Binary Golay Code. In standard code notation the codes have parameters [24, 12, 8] and [23, 12, 7], corresponding to the length of the codeword, the dimension of the code, and the minimum hamming distance between two codeword. An efficient implementation in the area of FPGA by using both Golay code (G23) and extended Golay code G(24) can be done by the help of different approaches of the encoding algorithm realizations. High speed with low-latency and less complexity in the design is the major concern at the time of working on FPGA. This paper presents a brief of Field Programmable Gate Array (FPGA) based design and simulation of Golay Code (G23) and Extended Golay Code (G24).

**Keywords**: FPGA, Golay Code, Extended Golay Code, Operational Delay.

## Introduction

There is every possibility that the signal transmitted gets corrupted by the noise existing in the channel. Hence, for error free communication along with the minimum power consumption as desired in the wireless channels, channels coding should be employed. This adds the bits and increases the length of the message. Hence, the coded message is called as code vector. At the receiver, these redundant bits are to be removed and the original message should be extracted, after using these bits for error checking. In this context, there are many types of coding techniques for error control for different type of channels for different types of applications. The recent trends in communication technology is to design the hardware with minimum chip area, should consume least power along with high speed decoding, best performance, approaching the maximum channel capacity. Coding Theory uses either a Hard-decision or Soft-decision based decoding for detecting and correcting data which has been encoded at the transmitter. The Hard-decision decoding uses data that has fixed values (‘0’ and ‘1’ in case of binary values) and compares against a threshold value to arrive at a decision of the data value whereas 26 Soft-decision decoder uses a complete range of values between the fixed values also to arrive for better estimation of the data .Hence, this scheme is better than hard decision scheme.

### Hard Decision

Assume that our communication model consists of a parity encoder, communication channel (attenuates the data randomly) and a hard decision decoder. The message bits “01” are applied to the parity encoder and we get “011” as the output codeword. The output codeword “011” is transmitted through the channel. “0” is transmitted as “0 Volt and “1” as “1 Volt”. The channel attenuates the signal that is being transmitted and the receiver sees a distorted waveform ( “Red color waveform”). The hard decision decoder makes a decision based on the threshold voltage. In our case the threshold voltage is chosen as 0.5 Volt (midway between “0” and “1” Volt). At each sampling instant in the receiver (as shown in the figure above) the hard decision detector determines the state of the bit to be “0” if the voltage level falls below the threshold and “1” if the voltage level is above the threshold. Therefore, the output of the hard decision block is “001”. Perhaps this “001” output is not a valid codeword (compare this with the all possible codewords given in the table above) , which implies that the message bits cannot be recovered properly.

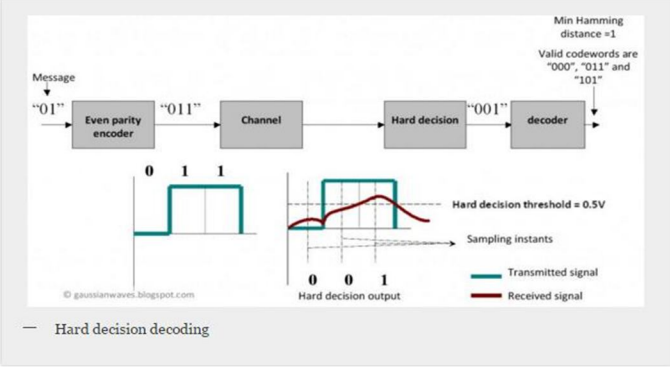


Fig 1 Hard decision decoder

**Soft Decision**

In Soft decision decoding, the received codeword is compared with the all possible codewords and the codeword which gives the minimum Euclidean distance is selected.

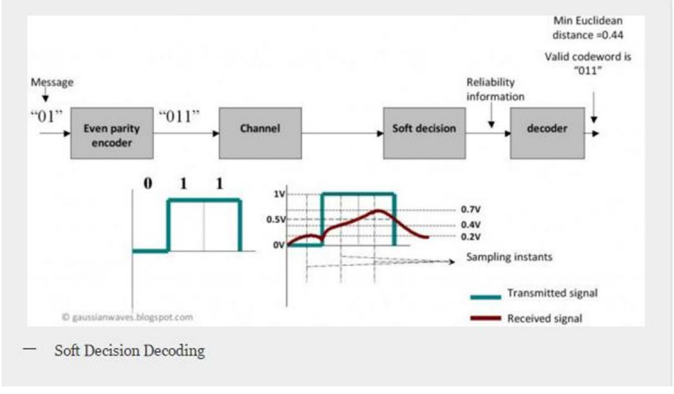


Fig 2 soft decision decoder

Thus the soft decision decoding improves the decision making process by supplying additional reliability information (calculated Euclidean distance or calculated log-likelihood ratio) Voltage levels of the received signal at each sampling instant are shown in the figure. The soft decision block calculates the Euclidean distance between the received signal and the all possible codewords The minimum Euclidean distance is "0.49" orresponding to "0 1 1" codeword (which is what we transmitted). The decoder selects this codeword as the output. Even though the parity encoder cannot correct errors, the soft decision scheme helped in recovering the data in this case. This fact delineates the improvement that will be seen when this soft decision scheme is used in combination with forward error correcting (FEC) schemes like convolution codes, Goley Code etc.

## Golay Code

The Golay code was presented in [1] to address error correcting phenomena. The binary Golay code (G23) is represented as (23, 12, 7), while the extended binary Golay code (G24) is as (24, 12, 8). The extended Golay code has been used extensively in deep space network of JPL-NASA as well as in the Voyager imaging system [6]. In addition, Golay code plays a vital role in different applications like coded excitation for a laser [4] and ultrasound imaging due to the complete sidelobe nullification property of complementary Golay pair. All these applications need generation of Golay sequence, which is fed as trigger to the laser modules. However, for generating Golay code an automatic pattern generator is used, which is of very high cost. To combat this problem, a hardware module programmed to yield a Golay encoded codeword may be used. Golay decoder is used extensively in communication links for forward error correction. Therefore, a high speed and high throughput hardware for decoder could be useful in communication links for forward error correction. There are two closely related binary Golay codes. The extended binary Golay code, G24 (sometimes just called the "Golay code" in finite group theory) encodes 12 bits of data in a 24-bit word in such a way that any 3-bit errors can be corrected or any 7-bit errors can be detected. The other, the perfect binary Golay code, G23, has codewords of length 23 and is obtained from the extended binary Golay code by deleting one coordinate position (conversely, the extended binary Golay code is obtained from the perfect binary Golay code by adding a parity bit.

## Literature Review

In **Pallavi Bhoyar [2016],** this paper focuses on the VHDL implementation of UART with status register which supports asynchronous serial communication. The paper presents the architecture of UART which indicates, during reception of data, parity error, framing error, overrun error and break error using status register. The whole design is functionally verified using Xilinx ISE Simulator [1].This brief lays out cyclic excess registration encoding plan and exhibits a productive execution of the encoding calculation in field programmable entryway cluster (FPGA) model for both the twofold Golay code (G23) and expanded paired Golay code (G24). Fast with low-dormancy engineering has been planned and executed in Virtex-4 FPGA for Golay encoder without fusing straight input shift register.

**In Manikandan J et al. [2016]**, in this paper, a novel attempt is made to design reconfigurable coder system which can be reconfigured on-the-fly to work either as an encoder, or decoder, or both encoder and decoder depending on the user requirements. In order to build the proposed reconfigurable system, Convolutional encoder, Viterbi decoder, Golay encoder and Golay decoder are employed in different combinations for the proposed design. The proposed systems are implemented on a Virtex-5 FPGA and the performance of the system with and without reconfigurable architecture are reported. It is observed that 56.36% of hardware resources and 72.21% of power are saved on using reconfigurable architecture over non- reconfigurable architecture. The proposed system can be easily extended to include various other encoding and decoding schemes [2].

In **Sindhuaja Muppalla et al. [2015],** this paper shows Universal Asynchronous Receiver Transmitter (UART), which is a kind of serial communication protocol. In parallel communication the cost as well as complexity of the system increases due to simultaneous transmission of data bits on multiple wires. Serial communication alleviates this drawback of parallel communication and emerges effectively in many applications for long distance communication as it reduces the signal distortion because of its simple structure. The UART implemented with VHDL language can be integrated into the FPGA to achieve compact, stable and reliable data transmission [3].

In **Satyabrata Sarangi et al. [2014],** this brief lays out cyclic excess registration encoding plan and exhibits a productive execution of the encoding calculation in field programmable entryway cluster (FPGA) model for both the twofold Golay code (G23) and expanded paired Golay code (G24). Fast with low-dormancy engineering has been planned and executed in Virtex-4 FPGA for Golay encoder without fusing straight input shift register [4]. This brief likewise displays an advanced and low-unpredictability interpreting design for broadened paired Golay code (24, 12, 8) in view of a deficient most extreme probability unraveling plan. The proposed engineering for decoder involves fewer zones and has lower idleness than a portion of the late work distributed here. The encoder module keeps running at 238.575 MHz, while the proposed design for decoder has a working clock recurrence of 195.028 MHz. The proposed equipment modules might be a decent possibility for forward mistake remedy in correspondence join, which requests a rapid framework.

Table 1: Summary of Literature Review

| Entitle of paper | Approac hed used | Softw are | Param eter | Published Year |
|---|---|---|---|---|
| Design of Encoder and Decoder for Golay code | Design Encoder and decoder using weight measure ment | Xilinx 10.1 i | Slice =305, LUT=598 | IEEE 2016 |
| Design and Implementa tionof Reconfigura ble Coders for Communication Systems | Design coded encoder and decoder | Xilinx 9.1 i | Slice =353, LUT=610 | IEEE 2016 |
| A Novel VHDL Implementa tion of UART with Single Error Correction and Double Error Detection Capability | Detected single input output bit | Xilinx 8.1 i | Slice =453, LUT=678 | IEEE 2015 |
| Efficient Hardware Implementa tionof Encoder and Decoder for Golay Code | Three bit measure ment | Xilinx 8.1 i | Slice =543, LUT=792 | IEEE 2014 |

Table 2: Comparison of the Decoder architecture considering Latency and Area

| Reference | Latency | Area (Number of Gates |
|---|---|---|
| [4] | 576 clock cycles | - |
| [11] | 23 gate level delay | 6000 |
| [7] | - | 3500 |
| [5] | 48 clock cycles | 4000 |
| [6] | 27 clock cycles | 3013 |
| proposed | 24 clock cycles | 2543 |

Table 3: Comparison of the Encoder Architecture considering Latency and LUT‟s

| Reference | LUT Utilization 12 (%) | Latency |
|---|---|---|
| [9] | 1.33 | - |
| [12] | 1.72 | 12 |
| [6] | 0.14 | 12 |
| Proposed | 0.12 | 12 |

## Binary Golay Code

Let G be the 12 × 24 matrix G = [$I_{12}$ | A], where $I_{12}$ is the
12 × 12 identity matrix and A is the 12 × 12 matrix. The binary linear code with generator matrix G is called the extended binary Golay code and will be denoted by G24.

Properties of the extended binary Golay code

- The length of G24 is 24 and its dimension is 12.
- A parity-check matrix for G24 is the 12 × 24 matrix

H = [A | $I_{12}$].
The code G24 is self-dual, i.e., G⊥ 24 = G24.

$$A = \begin{bmatrix} 0 & 1 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & \end{bmatrix}$$

- Another parity-check matrix for G24 is the 12 × 24 matrix H0 = [I12 | A] (= G).
- Another generator matrix for G24 is the 12 × 24
- matrix G0 = [A | I12] (= H).

- The weight of every codeword in G24 is a multiple of 4.
- The code G24 has no codeword of weight 4, so the minimum distance of G24 is d = 8.
- The code G24 is an exactly three-error-correcting code.

## Existing Methods For Encoding Algorithm

The Golay code is perfect nontrivial linear error correcting code. The representation of binary Golay code (G23) is (23,12,7) which presents length of codeword is 23 bits which describes the original 12-bit message. The minimum Hamming distance between any two Golay code words is 7. While the representation of extended Golay code (G24) is (24,12,8) which is obtained by adding one parity bit to the codeword. In extended Golay codeword codeword length is 24 bits describing the 12 bits message and the minimum hamming distance between the codeword is 8. The 24 bit Golay codeword is an extension of 23 bit binary Golay code. x11 + x9 + x7 + x6+ x5 + x1 + 1 and x11 + x10 + x6 + x5 + x4 + x2 + x1 are possible generator polynomials for Golay code. The coefficient of these two polynomials is C75h and AE3h.In this algorithm AE3h characteristic polynomial is considered in this algorithm. The remainder obtained at the end of long division process that gives the required check bits for Golay code. After Appending the generated check bits by using CRC generation process with massage bits gives the extended Golay code. The extended Golay code is the linear code and the parity check matrix for extended Golay code is 12 by 24 [I, B] where B is the 12 by 12 matrix. This code has distance 8 and so it will correct up to three errors. The matrics B which used for generating a parity check matrics for extended Golay code which is ginen below.

$$B=\begin{bmatrix}
1&1&0&1&1&1&0&0&0&1&0&1\\
1&0&1&1&1&0&0&0&1&0&1&1\\
0&1&1&1&0&0&0&1&0&1&1&1\\
1&1&1&0&0&0&1&0&1&1&0&1\\
1&1&0&0&0&1&0&1&1&0&1&1\\
1&0&0&0&1&0&1&1&0&1&1&1\\
0&0&0&1&0&1&1&0&1&1&1&1\\
0&0&1&0&1&1&0&1&1&1&0&1\\
0&1&0&1&1&0&1&1&1&0&0&1\\
1&0&1&1&0&1&1&1&0&0&0&1\\
0&1&1&0&1&1&1&0&0&0&1&1\\
1&1&1&1&1&1&1&1&1&1&1&0
\end{bmatrix}$$

The extended Golay code is obtained by appending a parity bit 1, if the weight of 555686h is odd (11). Hence the generated extended Golay codeword is (0101 01010101 1101 0000 1101).

Table 4 Extended Golay [24, 12] Codeword

| Parity bit | Check bit | Message bit |
|---|---|---|
| 1 | 110 1000 0110 | 0101 0101 0101 |

The weight of extended Golay code (G24) should be multiple of four and greater than equal to eight. The extended Golay code generated by the binary Golay code is unique three error correcting code. The extended Golay code has various practical applications for example voyager spacecraft mission.

## CRC Method for Check Bit Generation

The steps required to accomplish the encoding procedure are enlisted as follows.

1) A characteristic polynomial $G(x)$ is chosen for check bits generation.

2) 11 zeros are appended to the right of message $M(x)$, such that resultant polynomial $P(x)$ participates in long division process with $G(x)$.

3) The remainder bits except the most significant bit (MSB) resulted at the end of the division operation are the check

bits for *G*23. Appending check bits with the message gives us the the encoded Golay (23, 12, 7) codeword. A parity bit is added to convert the binary Golay code into extended binary Golay code (24, 12, 8). If the weight of binary Golay code is even, then parity bit 0 is appended, otherwise 1 is appended. The proposed encoder algorithm clearly follows the basic CRC generation process and includes a method for converting binary.

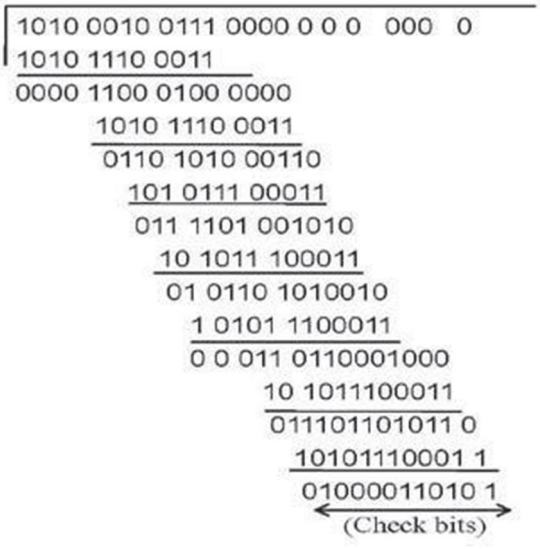


Fig3. Example of check bits generation

Golay code to extended Golay code before proceeding for designing architecture. An example of Golay code word generation based on the above mentioned algorithm is shown in Fig. 1. Let us say, the message to be encoded is A27h. Hence, $M(x)$ = A27h and $P(x)$ in binary format is represented as 1010 0010 0111 0000 0000 000. Finally, the generated check bits in hexadecimal format are 435h. Hence, the encoded codeword for the message bits (A27h) is A27435h. This is a binary Golay code word. To convert it into an extended Golay code, a parity bit 1 is appended, as weight of A27435h is 11 (odd). Finally, the generated Golay (24, 12, 8) codeword is (1010 0010 0111 1000 0110 101 1). The validity of the generated Golay code can be tested by measuring the weight of the code.

The weight of every *G*24 code should be a multiple of four and greater than equal to eight. The generated code word shown in the example has a weight of 12, which is a multiple of four and greater than eight. Hence, the generated code is valid and thus the algorithm.

## Soft Decision Decoder for G24

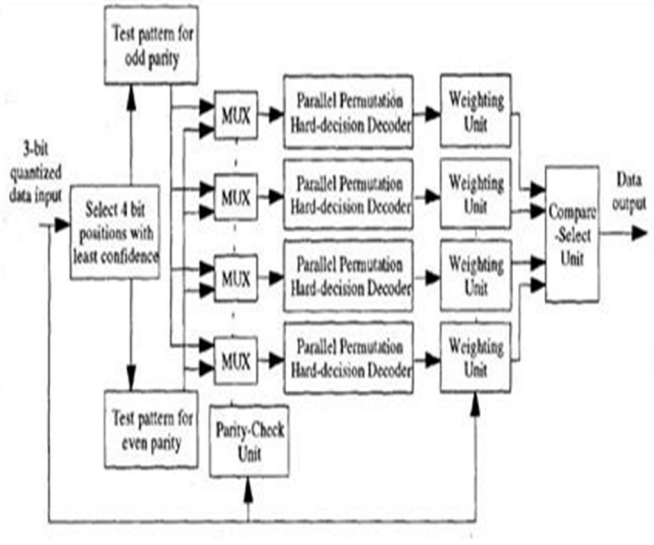


Fig.4 Soft decision decoder

## Module used for Golay Code

**LFSR Generation process**
To design encoder and decoder architecture using Golay code function create a key generation process based on polynomial equation. This equation is present in GALOIS field process and to update the key value in input data bits. The pseudo random pattern generator process is used to generate the pattern result based on
normalized result.

**CRC Generation process**
CRC generation process is a error detection process in encoding and decoding the data. In CRC generation process, the division operation occurs between input data bits and Polynomial bits. Our work is to modify the division operation architecture in encode and decode function. We apply the XOR gate operation in subtraction process and to design a priority based encoder design[3]. This design is to analysis the subtraction data bits and to add the no of '0' bits.

**Golay code generation process**
Golay code function is to add the addition key dating encoder operation. This process is to modify the data and key addition process. This function in mainly based on majority architecture design process. The 16-bit majority architecture used to the data encoding process and to modify the majority function using the Boolean logic function. This logic function to optimize the Boolean equation. This equation to reduce the gate component for the 16-bit majority architecture

**Decoder architecture**
First we collect the encoder output data bits and to modify the decoder architecture using extended Golay code architecture. This architecture is to analysis the overall encoder output data. Then to calculate the majority output data bits and to compare the Golay code architecture data bit location. Then to check the CRC key data bits. So we apply the CRC calculation process and to solve the final data bit in '0' level. Then to collect the original message data bits. The output bits are not equal to '0' level, so the error bits are present in receiving bits

**Encoder architecture**
This encoder architecture consist of GF based LFSR equation result, CRC architecture and Golay code architecture. This architecture is to modify the regular encoder structure and to update the key in every data transmission processing time. Data encoder operation is added the input message bits, CRC output key bits and GOLAY code architecture based majority bits. Then to transmit the encoder architecture data bits.

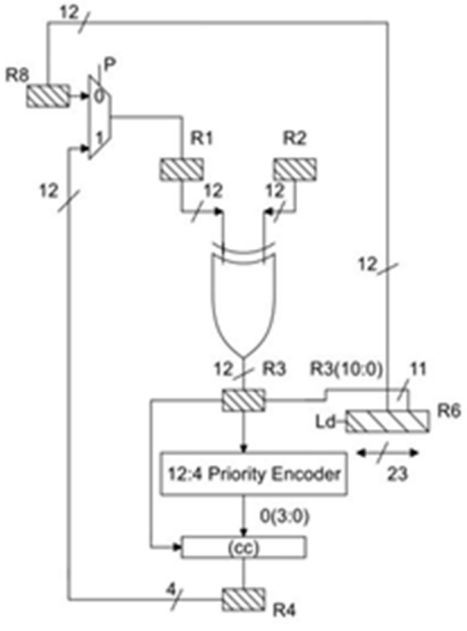


Fig. 5 Architecture for generating binary (23,12,7) Golay code [1]

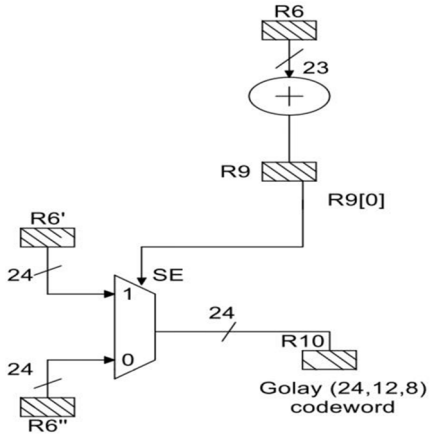


Fig. 6 Architecture to convert binary Golay code into extended Golay code [1]

## Proposed Methodology

- In each step during polynomial division, simple binary XOR operation occurs for modulo-2 subtraction. The residual result obtained at each step during the division process is circularly left shifted by number of leading zeros present in the result. A 12:4 priority encoder is used to detect efficiently the number of leading zeros before first 1 bit in the residual result in each step. A circular shift register is used to shift the intermediate result by the output of priority encoder. A 2:1 multiplexer is used to select the initial message or the circularly shifted intermediate result. The control signal used for the multiplexer and the controlled subtractor is denoted as *p*, which is bit wise OR operation of priority encoder output. A controlled subtractor is used for loop control mechanism.
- Initially, one input of subtractor is initialized with 11, which is the number of zeros appended in the first step of the long division process and it gets updated with the content of *R*7 register due to multiplexer selection after each iteration. The output of the priority encoder is the other input to the subtractor. After the final iteration, the result of subtractor is zero, which is stored in register *R*7. The register *R*6 is loaded when the content of register *R*7 becomes zero, which depicts the end of the division process and hence the check bits generation process.
- Architecture for decoding extended Golay Code consist of syndrome measurement, weight measurement, priority encoder and multiplexer to select the register. SatyabrataSarangi and Swapna Banerjee [1] proposed the structure of weight measurement unit that consists of 2-bit and 3-bit ripple carry adder. Ripple Carry Adder consumes large area and induces more delay as compared to Common Boolean Logic (CBL) adder and Kogge-Stone Logic (KSL) adder. Thus to overcome the mentioned problems we will use CBL and KSL in our model.

## Method of Design

1 Use of Cooman Boolean Logic (CBL) adder and Kogge-stone adder reduce area and delay of decoding algorithm.
2 Design 13:1 mux using 2:1 mux and 4:1 mux to reduce the delay.
3 Use of different binary Golay code is (23, 12, 7) and (24, 12, 8).
4 All the modules design to different device family i.e. Spartan-3, Vertex-4 and Vertex-7.

decoding algorithm have been successfully applied to short block codes such as Golay Code. Decoding algorithm consists of syndrome measurement unit, weight measurement unit and weight constraint. Table1 gives our approximated count of reduction in the number of gates resulting in minimizing the area and improved latency of 24 clock cycles in the Decoder Architecture. Also, Table 2 gives the approximated percentage (0.12%) of LUT utilization and improved Latency of the Encoder Architecture. The purpose of this paper is to review the published encoding and decoding models in the literature and to critique their reliability effects. We will try to reduce the area, Maximum Combinational Path Delay (MCPD) of decoding algorithm of Golay Code and to modify the majority function using the Boolean logic function. This logic function to optimize the Boolean equation. This equation to reduce the gate component for the 16-bit majority architecture.

## Expected Result

In this paper, the Golay Code and operation for various encoder and decoder is discussed. This encoding and decoding

algorithm have been successfully applied to short block codes such as Golay Code. Decoding algorithm consists of syndrome measurement unit, weight measurement unit and weight constraint. Table1 gives our approximated count of reduction in the number of gates resulting in minimizing the area and improved latency of 24 clock cycles in the Decoder Architecture. Also, Table 2 gives the approximated percentage (0.12%) of LUT utilization and improved Latency of the Encoder Architecture. The purpose of this paper is to review the published encoding and decoding models in the literature and to critique their reliability effects. We will try to reduce the area, Maximum Combinational Path Delay (MCPD) of decoding algorithm of Golay Code.

## Conclusion and Future Scope

In this paper, the Golay code and operation for various encoder and decoder is discussed. This encoding and decoding algorithm have been successfully applied to short block codes such as Golay code. Decoding algorithm consists of syndrome measurement unit, weight measurement unit and weight constraint.

The purpose of this thesis is to review the published encoding and decoding models in the literature and to critique their reliability effects. We will try to reduce the area, maximum combinational path delay (MCPD) of decoding algorithm of Golay code.

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